Hall Ticket Number:

Code No. : 12228 AS N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. II-Semester Advanced Supplementary Examinations, September-2023

Logic and Switching Theory

(Common to CSE & AIML)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Simplify the given Boolean function using Karnaugh map. $f(w, x, y, z) = \Sigma(0, 1, 4, 5, 6, 7, 9, 11, 15) + \Sigma_d(10, 14)$	2	2	1	1,2
2.	Define DeMorgans Theorem-1 and 2 along with a brief explanation.	2	1	1	1
3.	Find all the prime implicants for the following Boolean function and determine which are essential: $F(w,x,y,z) = \Sigma(2,3,4,5,6,7,9,11,12,13)$	2	2	2	1,2
4.	Draw the multiple level NAND circuit for the expression: $w(x+y+z)+xyz$	2	2	2	1,2
5.	Design a FULL ADDER circuit along with clearly specifying its truth table	2	3	3	1,2,3
6.	Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable and 2-to-4 line decoder.	2	3	3	1,2,3
7.	A certain flip-flop has four operations: set to 0, no change, complement, and set to 1 when inputs A and B are 00, 01, 10, and 11, respectively. a) Tabulate the characteristic table. b) Derive the characteristic Equation.	2	3	4	1,2,3
8.	Explain Ripple counters taking a 3 bit UP Counter example.	2	1	4	1
9.	List the similarities and differences between RAM and ROM	2	1	5	1
10.	The memory units that follow are specified by the number of words times and the number of bits per word. Give the number bytes stored in the memories listed below: a)16M*32 b)256K*64	2	1	5	1
	Part-B (5×8 = 40 Marks)				
11. a)	$f(w, x, y, z) = \Sigma(1, 2, 3, 5, 13) + \Sigma_d(6, 7, 8, 9, 11, 15)$ is a function. Find the minimal sum of products expression and also a minimal product of sums expression. Are the expressions same or different? Comment.	4	2	1	1,2
b)	Convert the following numbers with the indicated bases to decimal: a)$(10001.101)_2$ b)$(67AC.B)_{16}$	4	1	1	1

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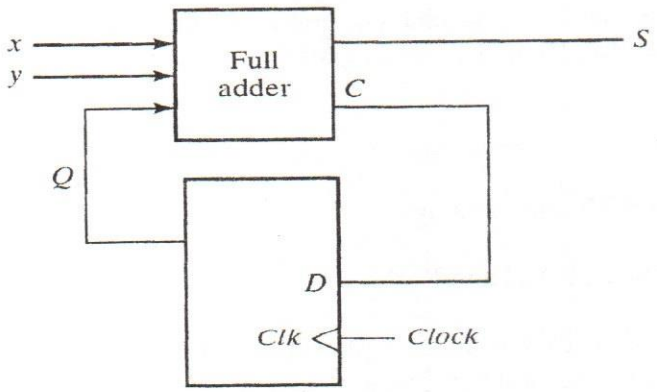
12. a)	Implement the function with OR-AND two level form: $F(A, B, C, D) = \Sigma m(0, 2, 3, 4, 7, 9, 15) + \Sigma_d (6, 8, 11)$	4	2	2	1,2
b)	Minimize the below function using Quine–McCluskey Tabular method, $f(A, B, C, D, E) = \Sigma (1, 5, 6, 7, 9, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 29, 30)$	4	3	2	1,2
13. a)	Construct a 4 bit comparator circuit with a neat diagram which has the three essential features (a) Equal (b) Less than (c) Greater than.	4	3	3	1,2,3
b)	Implement the following Boolean function with a 4*1 multiplexer and external gates. a) $F1(A,B,C,D)=\Sigma (1, 2, 4, 7, 8, 9,10, 11, 13, 15)$ b) $F2(A,B,C,D)= \Sigma(0,1,5,7,8,13,14)$	4	3	3	1,2,3
14. a)	Design a sequential Circuit with two JK flip-flops A and B and two inputs E and F.If E=0 the circuit remains in the same state regardless of the value of F. When E=1 and F=1 the circuit goes through the state transitions from 00 to 11, to10, to 01, back to 00 and repeats. When E=1 and F=0 the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00 and repeats.	4	3	4	1,2,3
b)	A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown below. Derive the state table and state diagram of the sequential circuit.  	4	3	4	1,2,3
15. a)	Using 64 * 8 ROM chips with an enable input, construct a 512 * 8 ROM with eight chips and a decoder.	4	3	5	1,2,3
b)	Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms. $A(x, y, z) = \Sigma (1, 3, 5, 6)$ $B(x, y, z) = \Sigma (0, 1, 6, 7)$ $C(x, y, z) = \Sigma (3, 5)$ $D(x, y, z) = \Sigma (1, 2, 4, 5, 7)$	4	3	5	1,2,3

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16. a)	Simplify the following Boolean expressions to minimum number of literals: a) xyz+x'y+xyz' b) xy+x(wz+wz')	4	2	1	1,2
b)	Implement the given function with NOR-OR two level form $f(A, B, C, D) = \Sigma m(0, 1, 4, 6, 8, 9, 10, 12)$	4	2	2	1,2
17.	Answer any *two* of the following:				
a)	Design a multiplier circuit capable of multiplying two binary numbers $B_3B_2B_1B_0$ and $A_3A_2A_1A_0$ using adders as building blocks.	4	3	3	1,2,3
b)	For the following state table	4	3	4	1,2,3

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	e	a	0	0
b	c	d	0	0
c	e	f	0	0
d	h	b	1	0
e	c	d	0	0
f	e	a	1	1
g	h	g	0	1
h	h	b	1	0

a)Tabulate the reduced state table

b)Draw the state diagram corresponding to the reduced state table

c)	Tabulate the PAL programming table and draw the fuse map for the combinational circuit that squares a three bit number.	4	3	5	1,2,3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	36%
iii)	Blooms Taxonomy Level – 3 & 4	44%

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